Modeling of Pulsed Laser Thermal Annealing for Junction Formation Optimization and Process Control

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Abstract

It is now a well known that the next generation devices in many fields of the semiconductor industry will be based on 3D architectures. In this framework, low thermal budget annealing technological solutions are required. For many applications, either in the field of sensors, microprocessors or high density memories, the Laser Thermal Annealing (LTA), an ultrafast and low thermal budget process, is one of the most promising solutions. This UV (308 nm) pulsed laser annealing process has already been adopted in production for the passivation step of BackSide Illuminated CMOS Imaging Sensors, and the contact formation step of power devices. During the annealing process, the high temperature region (e.g. over 1400 °C) needs to be restrained to very thin layers (from nm to µm range) while keeping the underlying fragile layers (metal and bonding) and devices at a lower temperature (e.g. less than 300 °C). In order to offer appropriate annealing solutions to the recent developments in 3D architectures, an accurate modeling of the LTA process is needed. In this work, the goal is to adapt the laser process parameters for various desired junction depths in silicon (Figure 1) conditioned by the multitude of applications. The junction formation is realized in a very fast process (sub-µs) involving melting and diffusion in liquid phase. Therefore, a transient model taking into account the silicon solid/liquid phase change is required. The process parameters that need to be optimized in order to reproduce the experimental data for various annealing conditions are the laser fluency (i.e. energy density) and the pulse shape (characterized by the pulse duration). In this paper we present recent results in LTA process modeling for melt depth control. An excellent agreement is found between simulation and experiment.
The advantage given by this modeling is the possibility to predict the effect of LTA parameters on the process. Potential applications for this tool are the process optimization, the process control software or the feasibility studies in case of new devices or process developments for various materials and applications.

Figures used in the abstract

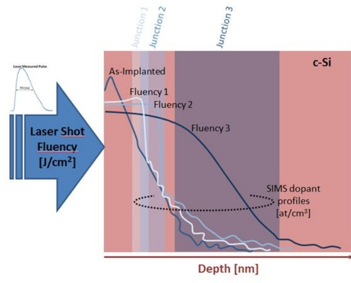

Fig. 1. LTA process schematic example for junction formation in crystalline silicon (c-Si). Melting Depth and junction abruptness depend on laser shot Fluency. Here, the difference between the melt velocity and the dopant diffusion one becomes visible for higher Fluencies.

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